ANALOG SIGNAL PROCESSING SOLUTION FOR IMAGE ALIGNMENT

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ABSTRACT

Imaging and Image sensors is a field that is continuously evolving. There are new products coming into the market every day. Some of these have very severe Size, Weight and Power constraints whereas other devices have to handle very high computational loads. Some require both these conditions to be met simultaneously. Current imaging architectures and digital image processing solutions will not be able to meet these ever increasing demands. There is a need to develop novel imaging architectures and image processing solutions to address these requirements. In this work we propose analog signal processing as a solution to this problem. The analog processor is not suggested as a replacement to a digital processor but it will be used as an augmentation device which works in parallel with the digital processor, making the system faster and more efficient. In order to show the merits of analog processing the highly computational Normalized Cross Correlation algorithm is implemented. We propose two novel modifications to the algorithm and a new imaging architecture which, significantly reduces the computation time.

KEYWORDS

Analog Signal Processing, Parallel Architecture, Image Alignment, Stereo Correspondence & Normalized Cross Correlation.

1. INTRODUCTION

The imaging and image sensor industry is going through a huge wave of change. Very soon there is going to be a great demand in the market for wearables like smart watches, headbands, glasses etc. Cameras will be an integral part of these devices. However these devices have severe Size, Weight and Power (SWaP) constraints. On the other hand companies are also trying to develop multi-megapixel sensors and there have been talks of developing gigapixel sensors for use in defence, space and medical applications. Collecting such huge amounts of data and processing it is not an easy task. There are a of lot emerging applications in the field of computer vision, biometric analysis, bio-medical imaging etc. which require ultra-high speed computations. Another area that is gaining traction is the use of stereo cameras, camera arrays and light-field cameras to perform computational imaging tasks. Current imaging architectures and digital image processing solutions will not work in all of these situations because they will not be able to handle the high computational loads and meet the SWaP requirements simultaneously. Hence there is a need for novel ideas and solutions that can address these requirements.

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In this paper we reintroduce the concept of analog image processing and present it as a solution to the above problems of reducing SWaP and high computational load. Generally the use of the term analog image processing has been restricted to film photography or optical processing. We are using neither of these approaches but we are performing analog signal processing by considering the image data to be a continuous stream of analog voltage values.

In order to show the advantages of analog processing we chose the problem of image alignment in stereo cameras. Image pairs captured from the stereo cameras can be used for a variety of purposes like constructing disparity and depth maps, refocusing, to simulate the effect of optical zoom etc. Image alignment can be used for stitching images to create panoramas, for video stabilization, scene summarization etc. Whatever the application, one of the most important steps in stereo image processing is to find correspondence between the points in the two images which represents the same 3D point in the scene. This has been an active area of research for many years now and there are a lot of stereo correspondence algorithms that have been developed. However some of these algorithms are either slow or have poor performance in the presence of noise or low light. The reason for these algorithms being slow is the very high computational requirement. In this work we pick one such stereo correspondence algorithm, Normalized Cross Correlation (NCC). NCC is very robust to noise and changes in the image intensity values but it is not preferred because of its high computational intensity. In this paper we propose two novel modifications to the algorithm which improves the computational speed without compromising the performance and also making it efficiently implementable in hardware. We also propose a new circuit architecture that can be used to implement the modified NCC algorithm in the analog domain. The analog domain implementation provides further speedup in computation and has lower power consumption than a digital implementation.

The organization of the paper is as follows. Section 2 gives a brief introduction to the NCC algorithm. Section 3 discusses the proposed modifications to the NCC algorithm. In section 4 a hardware circuit architecture for the implementation of the NCC algorithm is proposed. Experimental results are discussed in section 5. The work is concluded in section 6.

2. NORMALIZED CROSS CORRELATION

All stereo correspondence algorithms can be broadly classified into intensity based algorithms and feature based algorithms. In feature based algorithms features such as edges and contours are extracted from both stereo images and then a correspondence is established between them. In intensity based algorithms, blocks of pixels from one image are compared to blocks of pixels from other images and a similarity measure such as correlation or sum absolute difference is used to find the best matching block. Each of these algorithms have their own advantages and disadvantages. Both algorithms are used widely.

The Intensity based algorithms are very simple to implement, they are robust and they produce dense depth maps. They fail to perform well when the distance between the stereo cameras is too large or if there are rotations and shears in the stereo images. However the major drawback of the intensity based algorithms is that they are highly computational and hence it will be the algorithm of interest in this paper. In this study we address the issue of high computational load of the intensity-based algorithms through novel modifications to the algorithm and by the way of analog signal processing.

2.1. Review of Related Work

There has been a lot of research done on stereo image registration techniques as it relates to multiple fields like computer vision, medical imaging, photography etc. A variety of algorithms,

both feature based and intensity based have been developed. In [1], the author provides a survey of different image registration techniques used in various fields.

In this study we are mainly concerned with the implementation of an intensity based image alignment algorithm in hardware. There has been some work done in this regard but most of them are improvements to the old algorithms and some are digital hardware implementations of these algorithms.

In [2] Lewis proposes a fast normalized cross correlation algorithm, which reduces the computational complexity of the normalized cross correlation algorithm through the use of sum table methods to pre-compute the normalizing denominator coefficients. In [3] the authors take the fast normalized cross correlation algorithm one step further by using rectangular basis functions to approximate the template image. The number of computations in the numerator will then be directly proportional to the number of basis functions used to represent the template image. Using a smaller number of basis functions to represent the template image will certainly reduce the computation but it may give a bad approximation of the template image, which would result in poor image alignment. In [4] the author uses a pipelined FPGA architecture to perform the Normalized Cross Correlation operation. This increases the computation speed significantly.

There have been various other improvements and implementations of the NCC algorithm in literature however none of the implementations, to our knowledge, try to tackle the computational intensity problem of the normalized cross correlation algorithm from an analog signal processing perspective.

2.2. Reasons for Choosing Normalized Cross Correlation

There are a lot of intensity based stereo correspondence algorithms. We chose Normalized Cross Correlation (NCC) as the algorithm that we would implement because of the following reasons:

- 1. The images being aligned have translation in the X and Y direction but no rotation or shear. NCC algorithm performs well for such images.
- 2. NCC is less sensitive to variation in the intensity values of two images being aligned.
- 3. The NCC algorithm is computationally intensive. Hence it would be challenging to come up with methods to reduce the computation and make it implementable in real time or near real time and we believe analog signal processing would have a lot of value in such situations.

2.3. The General Algorithm

Template matching is one of the simplest methods used for image alignment. There are two images to be aligned. One image is called the template and the other image is called the reference. The template image is generally divided into blocks of smaller images. There is always a tradeoff between the depth accuracy that can be achieved and computation that can be handled in a NCC algorithm. Increasing the number of blocks by reducing the block size increases the accuracy to which depth can be estimated but it also increases the number of times the computations have to be performed. There is also a limit to which the block size can be reduced. If the block size is made too small then it might not have enough information to align with a matching block. Therefore choosing an optimum template block size is important.

Each template block is shifted on top of the reference image and at each point a correlation coefficient is calculated. This correlation coefficient will act as a similarity metric to identify the closest matching blocks.

The disadvantage of using cross correlation as a similarity measure is that it is an absolute value. Its value depends on the size of the template block. Also the cross correlation value of two exactly matching blocks may be less than the cross correlation value of a template block and a bright spot. The way around this problem is to normalize the cross correlation equation.

Equation (1) shows how the NCC algorithm is implemented [2].

$$C(u,v) = \frac{\sum_{x,y} [r(x,y) - \bar{r}_{u,v}] [t(x-u,y-v) - \bar{t}]}{\left\{ \sum_{x,y} [r(x,y) - \bar{r}_{u,v}]^2 \sum_{x,y} [t(x-u,y-v) - \bar{t}]^2 \right\}^{0.5}}$$
(1)

In the above equation \bar{t} represents the mean of the template image block and $r_{u,v}$ is the mean value of the reference image present under the template image block. The two summation terms in the denominator of the above equation represent the variances of the zero-mean reference image and template image respectively. Due to this normalization, the correlation coefficient is independent of changes to image brightness and contrast.

The denominator of the NCC equation can be calculated efficiently through the use of sum tables as suggested in [2]. However the numerator of the NCC is still computationally intensive. A direct implementation of the numerator of NCC algorithm on a template image of size $(T_x \times T_y)$ and a reference image of size $(R_x \times R_y)$ would require $(T_x * T_y)$ multiplications and additions for each shift (u,v). Reducing the template image size would reduce the number of computations per block but it will also increase the total number of blocks on which the NCC has to be performed.

3. MODIFICATIONS TO THE NCC ALGORITHM

In a general Normalized cross correlation algorithm the template image is divided into blocks and each block is shifted on top of the reference image. At each shift a normalized correlation coefficient is calculated. All the pixels in the block are used to perform this calculation as shown in equation (1). Once this is done for all shifts, a best matching block is picked and all the pixels in the template block are assigned the same shift/disparity value.

In the worst case scenario where there is no information available about the camera system or the scene, a brute force approach has to be used where the template image blocks have to be shifted all over the reference image. The computational complexity in this case would be very high. When some information is available about the camera system the maximum disparity that will be observed can be calculated and hence the number of shifts can be restricted. However this does not address the fact that the number of computations that have to be performed per block for each shift is still high.

A pre-processing step that is generally used in most stereo correspondence algorithms is image rectification. Image rectification projects stereo images onto a common reference plane so that the correspondence points have the same row coordinates. This essentially transforms the 2D stereo correspondence problem to 1D. However the rectification process itself will add to the computational complexity of the algorithm.

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In order to further reduce the computation and address the above mentioned issues we decided to use only the diagonal elements of the template image block and the reference image blocks to compute the correlation coefficient. All the other steps in the algorithm are followed as given by equation (1). The thought behind this approach is that the diagonal elements of a block have enough information to calculate the disparity. By introducing this modification we have effectively converted the problem of 2D NCC operation to a 1D NCC operation. This is very similar to the image rectification operation but since we are choosing only the diagonal elements we introduce two advantages both of which contribute to the reduction in computation.

- 1. We are not using an algorithm to reduce the NCC operation from 2D to 1D, it is a natural result of the data selection process and hence it does not involve any additional computations.
- 2. Since we are choosing only the diagonal elements, the number of computations per block is reduced to a great extent i.e. if we have a template image of size $T_x \times T_y$ the total computations per block in the numerator now reduces from $(T_x \times T_y)$ additions and multiplications to only $T_x(=T_y)$ additions and multiplications per shift. This reduction in the computation is even more significant when the template and reference image sizes are very large.

Another advantage of the modified NCC algorithm is in situations where the information of the camera systems capturing the images is not known and brute force shifts have to be applied. This modified algorithm will be a good solution for such cases.

In some pathological cases the images or particular template blocks might not have a lot of features like edges and contours or the features may all be located on the upper or lower triangular side. In such situations just using the diagonal elements to perform the NCC algorithm might not work. The solution to this problem may be as simple as using the off-diagonal elements instead of the diagonal elements. However in most practical applications we always have images with some features on the diagonal element so using all the pixels in a template image block is unnecessary as it will only add to the computation without producing any significant improvements in the results.

4. HARDWARE ARCHITECTURE

In a standard CMOS image sensor there are photodiodes that produce electrons proportional to the amount of light intensity that strikes them. This is then converted into voltage levels which are read out by the readout circuitry. In order to remove noise, a process called correlated double sampling (CDS) is used. After this the signals are amplified. All this happens in the analog domain. These signals are then digitized using analog-to-digital converters (ADCs) and stored in memory or are sent to digital processors for further processing. So the signal for the most part is in the analog domain and we can utilize this to our advantage to perform analog processing.

With this in mind we have come up with a new imaging architecture which would best utilize the features of both analog and digital domains. Figure 1 shows a top level block diagram of the proposed architecture. In this architecture we have the digital system accessing the sensor and it is pre-processing, digitizing and storing the images in memory as before. However we now have an analog system that is accessing the analog data on the sensor, processing it and then feeding it into a digital machine for any further computations. By doing this we have separated the process of image acquisition which is being done by a digital system and image processing which is being done by an analog system. The biggest advantage of such an architecture is that they are operating in parallel i.e. the image acquisition is independent of the processing. This is not true in the case of completely digital systems. In a fully digital system the image processing operation cannot

start until the images have been completely acquired and stored in memory. In this hybrid system the analog block is performing the computationally intensive task of running the NCC algorithm as and when the image data is being read off the sensor. This means that by the time the digital system has acquired the images the analog processor would have finished its computation and the outputs will be ready to be used by the digital system.

Another important point to be noted is that the analog processing block is not in the signal plane but in the control plane. One of the biggest disadvantages of an analog system is the amount of noise added by it. However in this kind of an architecture the analog block is not responsible for signal acquisition and hence the problem of signal being corrupted by noise vanishes immediately.

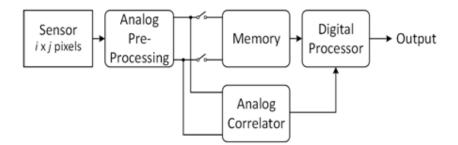


Figure 1: Proposed Architecture for the new Imaging systems

4.1. Implementing the modified NCC algorithm

Figure 2 shows the implementation of the modified NCC algorithm in the new imaging architecture. We have a digital system (shown on the left) which is accessing the sensor data, pre-processing, digitizing and storing it in memory. We have N analog channels which read the analog data from the sensor directly.

These N analog channels can be grouped into pairs in which one (odd numbered) channel is used to read the reference image data and the other (even numbered) channel is used to read template image data. The CMOS image sensors are capable of accessing individual pixel data. The readout circuitry is used to selectively read the diagonal elements of template and reference image blocks. Once the analog data has been read from the sensor we have it available to perform the NCC algorithm. According to eq. (1) in order to perform the NCC algorithm we first need a zero mean template image and zero mean reference image. In the case of digital systems it is not hard to compute the zero mean images from stored information. However in the new architecture we are directly accessing the analog data from the sensor and we would have to wait for an entire block of data to be read out in order to compute the mean and subtract it from the original signal. This would be a waste of processing time since this has to be done multiple times *i.e.* for each image block. In order to get around this problem we propose a second modification to the NCC algorithm. Here we use moving averages instead of regular averages and the moving average is subtracted from the original signal. The moving average circuit can be implemented as a low pass filter. The analog data from the sensor is passed through the moving average filter, the output of which is subtracted from the original signal. This is then fed to the multiplier and integrator which together perform the correlation operation. This calculates the numerator of the NCC algorithm. For calculating the denominator we plan to use the sum table method. This can be done efficiently by a digital system. So once the numerator calculation is done the analog signal is sampled and then fed into a DSP which normalizes the numerator and performs the decision making. The output will be disparity values in the X and Y direction. We also ran MATLAB simulations to

ensure that a change from an actual zero-mean image to one with moving averages does not affect the performance of the NCC algorithm.

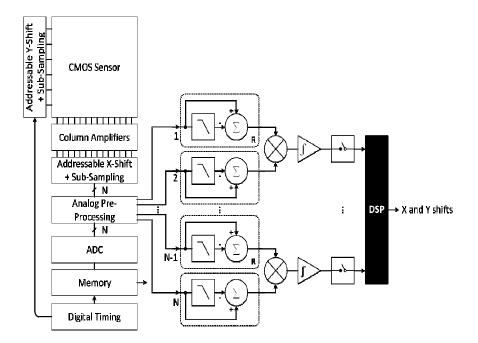


Figure 2: Implementation of NCC algorithm in the new Imaging architecture

5. EXPERIMENTAL RESULTS

In this section we compare the performance of the modified NCC algorithm to the original algorithm to show that the modified algorithm is faster and has a performance similar to the original algorithm. Since the modified algorithm has been developed to be implemented in analog hardware various other simulations are run that measures the performance of the modified algorithm.

We have run simulations on 15 sets of unrectified, grayscale stereo image pairs. These images have been captured under different illumination conditions which include incandescent light (In_Incd), outside bright light (Out_brt), outside low light (Out_clds), outside mixed shade lighting (Out_mxdshd). This allows us to test the performance of the algorithm in a more robust manner. All simulations have been done in MATLAB.

5.1. Cropping the template image

The stereo cameras have overlapping fields of view but the amount of overlap depends on the distance between the centres of the two cameras. In this work we have considered cameras whose centres are 6.5mm apart. Their hyperfocal distances are 70cm which means that all objects which are 35cm and beyond are in sharp focus. Since the distance between the centres are 6.5mm there will be some points in the scene that will be present in one of the images but not in the other. These points cannot be used for alignment and hence one of the images (template image) is cropped around the edges.

5.2. Evaluating the performance of the algorithms

The performance of the image alignment algorithms can be evaluated in a variety of different ways. Here the correlation coefficient is used as a performance measure. Once the final disparity values for all the template blocks are obtained, each template block is shifted by the disparity values obtained for that block. In order to get a uniform disparity variation across the entire image an interpolation technique is used. At the end of this process the two stereo images have been aligned. The correlation coefficient is calculated between the two aligned images and it is used as an indicator of the performance of the algorithm.

Figure 3 shows a comparison of the correlation coefficients obtained for 15 stereo image pairs by using the original NCC algorithm and the modified NCC algorithm. Each stereo image pair has a size of 1080x1920 pixels. The cropping of the template image around the edges is not more than 10% of the entire image size. The template block size chosen here is 128x128 pixels. As can be seen from the figure the performance of the modified NCC algorithm is very close to the original NCC algorithm. The performance was also tested for various other template block sizes and uniform performance was obtained for all. A speedup of 2x in MATLAB run time was observed for the modified NCC algorithm.

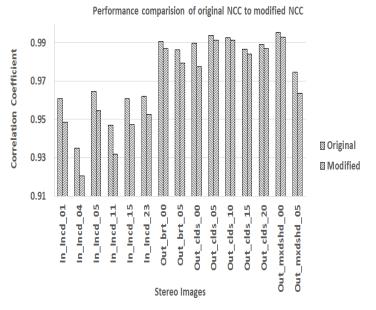


Figure 3: Performance comparison of the original NCC algorithm to modified NCC algorithm

It has to be noted that the objective of the above simulation is to compare the performance of the algorithms and not the digital and analog implementation of the algorithms.

Another performance measure that was used was the percentage improvement in the correlation coefficient values of the stereo images before and after alignment. Figure 4 shows these results. As it can be seen there is significant improvement in the correlation coefficients for all the images. It must be noted that for some images we see a very low percentage improvement. This is not because of the performance of the algorithm but because the input images were themselves almost aligned before the algorithm was applied.

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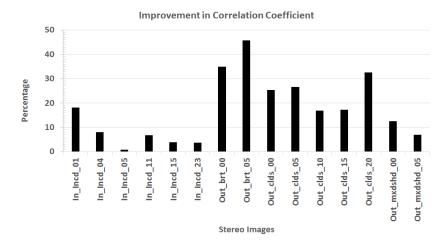


Figure 4: Percentage improvement in the correlation coefficient after alignment using modified NCC algorithm

As an example of the performance the modified NCC algorithm two figures 5 and 6 are shown. Figure 5 shows an overlap of a pair of stereo images before alignment. The areas of magenta and green show the areas of misalignment between the two images. The correlation coefficient measured for these two images before alignment is 0.7247. Figure 6 shows the overlap of two images after aligning them using the modified NCC algorithm. As can be seen from the figure there is hardly any misalignment between the two images. The correlation coefficient observed in this case is 0.9923.



Figure 5: Overlap of two stereo images before alignment



Figure 6: Overlap of the two stereo images after alignment

Figure 7 and Figure 8 shows the disparity variation for the image shown in figure 5 and 6 in X and Y direction respectively. These disparity values have been obtained through the modified NCC algorithm. The disparity values have been colour coded and the colour bar indicates the different disparity values. The disparity values vary from 18 to 33 for Figure 7 in the X (horizontal) direction. The disparity values vary from 43 to 53 for Figure 8 in the Y (vertical) direction.

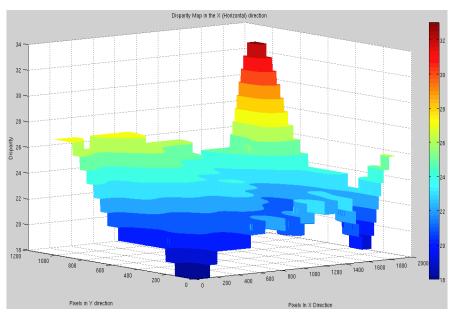


Figure 7: Disparity variation in the X(Horizontal) direction

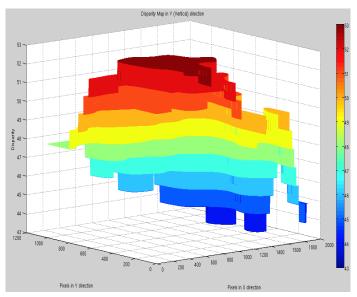
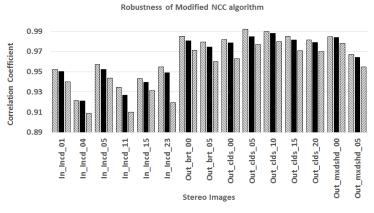


Figure 8: Disparity variation in the Y(Vertical) direction

5.3. Measuring the robustness of the modified NCC algorithm

We know that the NCC algorithm is robust to changes in the intensity values of the images. Here we try to measure the robustness of the modified NCC algorithm to changes in intensity values by changing the intensity values of one of the two stereo images. In the first case we reduced the intensity values of the template image by 90% uniformly across the image and used the modified NCC algorithm to align the images. This analysis addressed the fact that the illumination of a scene might change between the capture of two stereo images and the change in illumination was assumed to be uniform. However there might be rare situations where illumination on parts of the intensity values of the template image and analysed the performance of the modified NCC algorithm under these conditions as well. Figure 9 shows the results of these analyses. As it can be seen the modified NCC algorithm is very robust to changes in the image intensity values.



⊠ Original Intensity Values ∎ Uniform Intensity Variation ⊠ Random Intensity Variation

Figure 9: Robustness of the modified NCC algorithm to changes in image intensity values

Since the algorithm has been developed to be implemented in analog hardware it is very important to characterize the performance of the algorithm in the presence of noise. The two analog circuits that have been considered to be the primary contributors of noise are the multiplier and the integrator. In order to simulate the addition of noise by analog circuitry we first find the RMS value of the image intensity values. We multiply this RMS value by a number which indicates the percentage of noise being added by the circuit. This value is then multiplied by a random number picked from a Gaussian distribution. The outcome of this process is a noise value which is then added to the original image intensity. In our simulations it was found that the algorithm is more sensitive to the noise added by the multiplier than that by the integrator. Hence we maintain the noise added by the integrator at 20% and vary the amount of noise added by the multiplier. Figure 10 shows this performance variation. We have shown the performance for 3 different noise values added by the multiplier, 1%, 10% and 20%. As it can be seen the performance of the modified NCC algorithm is still good in the presence of noise added by the analog circuitry.

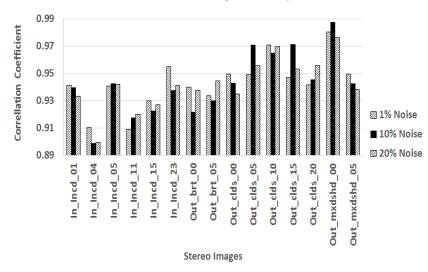




Figure 10: Performance of the modified NCC algorithm in the presence of Noise

5.4. Dynamic Range requirements and Power analysis

The amount of noise that can be tolerated by a circuit determines the dynamic range requirements for that circuit. The noise analyses done above will give us an idea of the dynamic range requirements for the analog circuits to perform the NCC operation. Analog circuits can easily achieve dynamic ranges of 40dB. This corresponds to a noise level of 1%. From Figure 10 we see that the modified NCC algorithm has excellent performance for a noise level of 1%.

The dynamic range requirements also dictates the power consumptions for analog circuits. The 4 major analog circuits required to implement the modified NCC operation are the low pass filter, analog summer, multiplier and integrator. We have performed initial circuit simulations for these components. Table 1 shown below gives approximate values of the power consumption for these components calculated for a dynamic range of 40dB based on these simulations. Here we assume that we have 64 analog channels in the architecture shown in Figure 2 and the number of components required are calculated based on that. The actual power consumptions can only be obtained once the components are realized and integrated.

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Component	Quantity	Power Consumption
LPF	64	$2.8 \text{mW/LPF}^{*}64 = 179.2 \text{mW}$
Summer	64	0.549mW/sum*64=35.13mW
Multiplier	32	1.83μ W/mul*32 = 0.058mW
Integrators	32	0.024mW/int*32 = 0.768mW

Table 1: Approximate power consumption values for the analog circuits

The total power consumption by the analog circuitry is 215.15mW. Based on some of the digital implementations such as [11] and [12], we see that the power consumption for an analog implementation will be very low compared to that of a digital implementation. This shows that we have significant power savings as well.

5.5. A Note on Computation Time

The modifications proposed to the NCC algorithm contribute to a significant reduction in the computation of the algorithm. Simulation results show a 50% reduction in computation time for the modified NCC algorithm over the original algorithm. The other factors which add to the reduction of computation time are the novel imaging architecture and analog processing. In the new imaging architecture the analog processor works in parallel with the digital acquisition system and hence it does not have to wait for the entire image to be acquired before the processing starts. By the time the acquisition is done the analog processor would have finished its computation time. The implementation of the NCC algorithm is being done in analog hardware. The analog processor is not limited by the data converters (ADCs) or logic delays. The settling times of well-designed analog circuits are very small. Hence an analog implementation of the NCC algorithm would be faster than a digital implementation and would contribute towards a further reduction in computation time.

6. CONCLUSIONS

In this work we propose analog signal processing as a solution for handling the high computational load of some of the image processing algorithms while simultaneously meeting the reduced SWaP requirements. The analog processor will be used to augment the digital processor and work in parallel with it to perform key computations, making the system faster and more efficient. We implement a highly computational stereo correspondence algorithm to align stereo image pairs. Two novel modifications were proposed to the NCC algorithm which reduced the computation and made the algorithm efficiently implementable in analog hardware. The modified algorithm has a 50% reduction in MATLAB computation time over the original algorithm. The actual analog hardware implementation of the algorithm and the new imaging architecture will contribute to a further reduction in computation time as compared to a digital implementation. An approximate power consumption of 215.15mW for obtained for the analog correlation block. Various other simulations were also run to check the robustness and performance of the algorithm. The experimental results obtained are very promising and we believe analog processing will be a viable solution to these problems. As a part of the future work and as a proofof-concept the analog image correlator circuit will be built from commercially available off the shelf components. A test plan will be setup for this circuit. Once the required results are obtained, the next step will be to build the architecture in silicon.

REFERENCES

- [1] Brown, L, (1992) "A survey of image registration techniques", ACM Journal (CSUR), Vol. 24, Issue 4, pp325-376.
- [2] Lewis, J.P. (1995) "Fast Normalized Cross Correlation", Industrial Light & Magic.
- [3] Briechle, Kai, & Uwe D. Hanebeck, (2001) "Template matching using fast normalized cross correlation", Aerospace/Defense Sensing, Simulation, and Controls. International Society for Optics and Photonics.
- [4] Radhamani & R, Keshaveni, (2012) "FPGA implementation of efficient and High speed template matching module", IJRTE, Vol. 2, Issue- 2.
- [5] Khaleghi, B et al. (2008) "A new Miniaturized Embedded Stereo-Vision System (MESVS-I)", CRV, pp26-33.
- [6] Gupta, N, (2007) "A VLSI architecture for Image Registration in Real Time", IEEE Transactions on VLSI systems, Vol. 15, Issue 9, pp981-989.
- [7] Roma, N et al. (2002) "A comparative analysis of cross-correlation matching algorithms using a pyramidal resolution approach", INESC Portugal.
- [8] Adhikari, G. et al. (2012) "Fast normalized cross correlation with early elimination condition", IEEE Transaction, ICRTIT 2012, pp136-140.
- [9] Tsai, Du-Ming & Chien-Ta Lin, (2003) "Fast normalized cross correlation for defect detection", Pattern Recognition Letters 24.15, pp2625-2631.
- [10] Szeliski, R, (2004) "Image Alignment and Stitching: A tutorial", Technical Report, Microsoft Research, Microsoft Corporation, MSR-TR-2004-92.
- [11] Ttofis, C., & Theocharides, T. (2012) "Towards accurate hardware stereo correspondence: A realtime FPGA implementation of a segmentation-based adaptive support weight algorithm", In Proceedings of the Conference on Design, Automation and Test in Europe, pp703-708.
- [12] Xiaotao Wang & Xingbo Wang, (2009) "FPGA Based Parallel Architectures for Normalized Cross-Correlation", 1st International Conference Information Science and Engineering (ICISE), pp225-229.
- [13] San Yong, Y., & Hon, H. W. (2008) "Disparity estimation for objects of interest", World Academy of Science, Engineering and Technology, 43.

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Dev V. Gupta received his Ph.D. in 1977 from the University of Massachusetts, Amherst. He held various engineering positions at the Bell Laboratories in Andover, MA, from 1977 to 1985. He was the General Manager at Integrated Network Corporation, a manufacturer of DSL access products, from 1985 to 1995.

Dr. Gupta founded two companies, Dagaz Technologies and Maxcomm, which were acquired by Cisco Systems in 1997 and 1999 respectively. These companies developed and manufactured telephone exchange and voice and data equipment for

DSL. He was Cisco's VP of Architecture in the access business unit between founding Dagaz Technologies and Maxcomm. In 2000, he founded Narad Networks which manufactured Gigabit Ethernet networking equipment for the cable industry. Narad Networks (renamed PhyFlex) was acquired by Cienna in 2007. Newlans was founded in 2003. He is a Charter Member of the Atlantic chapter of the Indus Entrepreneurs (TIE), an organization which promotes entrepreneurship. The World Economic Forum named him a 'Tech Pioneer' for the years 2001 and 2002. He is a Trustee of the University of Massachusetts, Amherst and a board member of the UMass Foundation. He is an Adjunct Professor at the University of Massachusetts where he created the Gupta Chair in the Department of Electrical and Computer Engineering. He has over thirty patents in communications, networking, circuit design, and signal processing. Dr. Gupta is the President and CEO of Newlans and he provides technical vision for the Company.

Jai Gupta currently serves as Chief Architect for commercialization efforts of Newlans' analog integrated circuits and wideband signal processing technology. His primary role is system architecture design and program management. He has previously held research positions at the National Institute of Standards and Technology and Huntington Medical Research Institute, worked as a systems engineer at metropolitan adhoc networking startup Windspeed Access, and held internship positions at broadband cable startup Narad Networks as well as Cisco Systems.

Jai recently completed the Executive MBA degree at Duke University's Fuqua School of Business with a concentration in Entrepreneurship and Innovation. He previously obtained the MSEE degree in Electrical Engineering Systems from the University of Southern California's Viterbi School of Engineering and the BSEE degree from the University of Pennsylvania's Moore School of Electrical Engineering.

